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	Application No.	Applicant(s)	
A) (1	10/710,724	KANG ET AL.	
Notice of Allowability	Examiner	Art Unit	
	Russell M. Kobert	2829	
The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this apport or other appropriate communication GHTS. This application is subject to	plication. If not include will be mailed in due o	ed course. THIS
1. 🖾 This communication is responsive to the Application filed 3	<u>0 July 2004</u> .		
2. The allowed claim(s) is/are <u>1-42</u> .	•		
3.	been received. been received in Application No cuments have been received in this of this communication to file a reply ENT of this application. itted. Note the attached EXAMINER as reason(s) why the oath or declara t be submitted. on's Patent Drawing Review (PTO- as Amendment / Comment or in the Comment or in the Comment of the drawing he header according to 37 CFR 1.121(content).	national stage applicate complying with the required and the requirement. S AMENDMENT or Notion is deficient. 948) attached Office action of the diagram of the diagram of the submitted. Note the submitted of	uirements OTICE OF
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal P 6. ☐ Interview Summary Paper No./Mail Dat 8), 7. ☐ Examiner's Amendr 8. ☑ Examiner's Stateme 9. ☐ Other	(PTO-413), te ment/Comment	

Application/Control Number: 10/710,724

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Reasons For Allowance

1. The following is an examiner's statement of reasons for allowance:

A method for monitoring stress-induced degradation of an insulation layer of a substrate having first and second conductive layers (or in the alternative, of an inter layer dielectric disposed between an upper layer interconnection line and lower layer interconnection line) comprising the steps of applying a first voltage to the first conductive layer (or upper layer interconnection line), the first voltage being a swing time dependent DC ramping voltage then measuring a first leakage current flowing through the first conductive layer (or upper layer interconnection line) to calculate a first proportional value followed by applying a second voltage to the first conductive layer (or upper layer interconnection line), the second voltage being a swing time dependent DC ramping voltage then measuring a second leakage current flowing through the first conductive layer (or upper layer interconnection line) to calculate a second proportional value further followed by the step of calculating a first ratio of the second proportional value to the first proportional value as further described in claim 1 or in the alternative, claim 23, has not been found.

It is further noted that the examiner's reasons are understood to be predicated upon consideration of each of the claims as a whole, and not upon any specific elements of the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably Application/Control Number: 10/710,724

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accompany the issue fee. Such submissions should be clearly labeled "Comments on

Statement of Reasons for Allowance."

2. The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

Chakravarti et al (U.S. Patent 4542340), Okada (U.S. Patent 6326792), Satoh et

al (Stress Induced Leakage Current of Tunnel Oxide Derived from Flash Memory Read-

Disturb Characteristics, Proc. IEEE 1995 Int. Conference on Microelectronic Test

Structures, Vol. 8, March 1995, pg. 97-101) and Tao et al (Fast wafer level monitoring of

stress induced leakage current in deep sub-micron embedded non-volatile memory

processes, 2002 IRW Final Report, 2002 IEEE, pg. 76-78) show methods for

characterizing leakage current integrity of a substrate having first and second

conductive layers such as non-volatile memory devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell Kobert whose telephone number is (571) 272-1963.

The Examiner's Supervisor, Nestor R. Ramirez, can be reached at (571) 272-2034.

For an automated menu of Tech Center 2800 phone numbers call (571) 272-2800.

Russell M. Kobert Patent Examiner

Group Art Unit 2829

November 23, 2005

PRIMARY EXAMINER

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